# CMSC 313 Spring 2024
# Quiz 4 - Answers

Full Name _____ Student ID _____

Questions on this quiz are either short response of true or false. Please print your answers clearly.

**Exercise 1.** (3 pts) If the width of the "read address" bus into a register file is 7 bits wide, at most how many registers can be stored in the register file?

$2^7 = 128$ : either of these is fine

**Exercise 2.** (3 pts) True or false: the width of a register file's "write address" bus is dependent on the number of bits per register.

False

**Exercise 3.** (3 pts) True or false: for a register file that has 1 data-in bus and 2 data-out buses, 1 register can be read from while 2 registers can be written to in the same cycle.

False

**Exercise 4.** (3 pts) Assume a register file uses a RAW (read after write) system. The current value of register 3 is 0x300 and register 4 is 0x400. If I write the value 0x200 to register 3, and read from register 3 and 4 in the same cycle, what will I read from the contents of register 3 and 4?

Register 3: 0x200, Register 4: 0x400

**Exercise 5.** Assume you are given a SIPO (serial-in parallel-out) register that can store $n$ bits. How many clock cycles would it take to completely

a. (3 pts) read to the register?

1

b. (3 pts) write to the register?

$n$

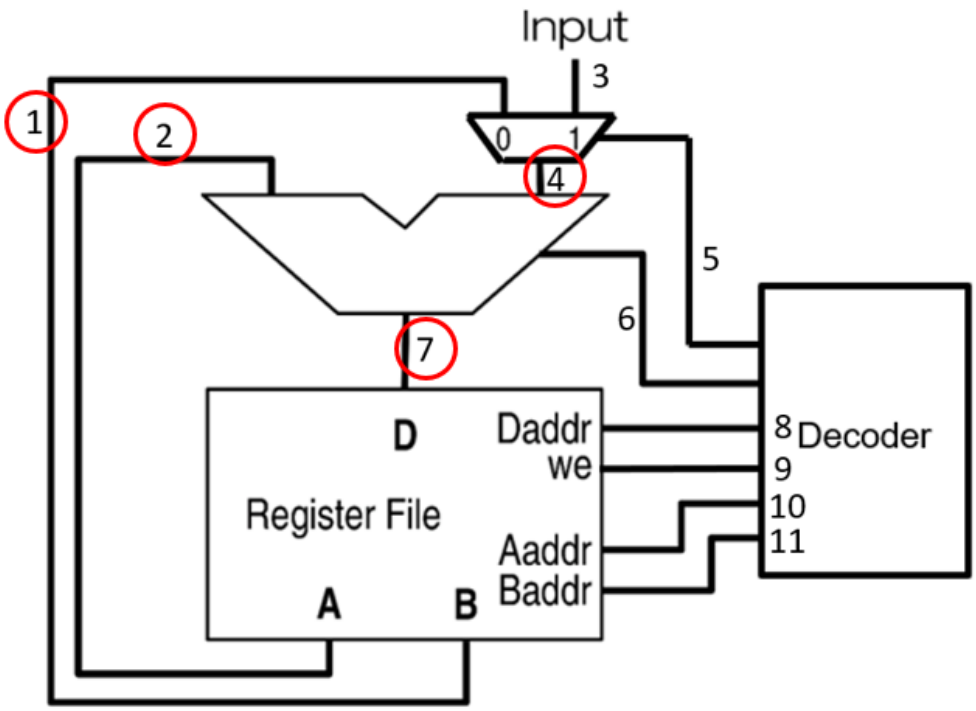
**Exercise 6.** (3 pts) What happens to PC (the program counter) when the zero flag is set to 1 and the carry flag is set to 0 and a "`BZS #32`" (Branch to address 32 if zero set) instruction is executed?

Full credit for "$PC = 32$" OR "the program points to address 32".
Partial credit for "the branch is taken"

**Exercise 7.** (3 pts) Given the previous example, what will the zero flag and carry flag be set to after the statement is executed?

unchanged. Zero flag=1, Carry flag=0

**Exercise 8.** (3 pts) Circle all numbers labeled on the wires that carry actively used data (not addressing or control) when an instruction that uses non-immediate inputs is executed.




**Exercise 9.** True or false: In the 64-bit x86 architecture:

a. (3 pts) there are 8 general purpose registers.

false

b. (3 pts) the RSP register points to the top of the stack.

true

c. (3 pts) the RSP register is 64 bits wide.

true

**Exercise 10.** (4 pts) In the 64-bit x86 architecture, The RAX register is initially set to 0. If I set the AX register to 0x0123, what is the value of the AL register?

0x23